Faculty of Electrical Engineering, Banja Luka



WISHBONE I2C IP CORE

USER MANUEL

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# **Introduction**

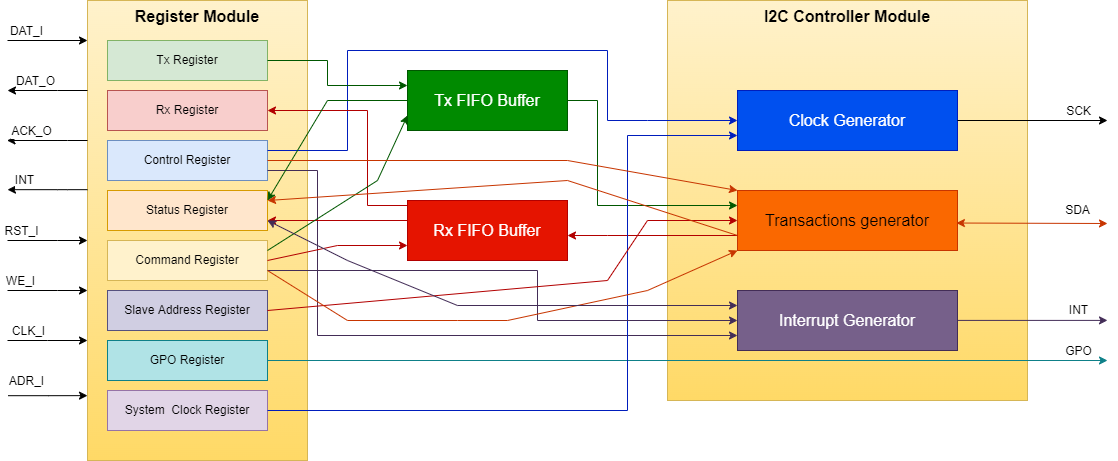
This document is meant to be a guide for future users of *Wishbone I2C IP CORE*. This document will explain how to access, configure and use I2C IP Core.

Wishbone I2C IP Core is designed to enable connection of Wishbone Transaction Generator on one side and I2C Test Device on the other side. Wishbone I2C IP Core si responsible for communication between them. Wishbone Transaction Generator sends data and comands that will let I2C IP Core know what to do with data (store into TX Fifo Buffer, read from RX Fifo Buffer, Start Transaction, ...). Also Wishbone Transaction Generator is used to configure I2C IP Core.

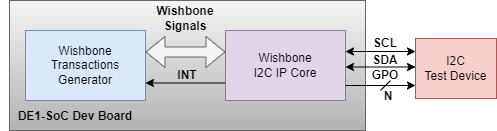
# **Specification**

* Supported receive and transmit FIFO buffer with depth of 16 elements
* Desing is compatible with I2C Standard
* Supported Master and Slave mode
* Supported generation and detection of ACK bit
* Supported generation and detection of START Condition
* Supported generation and detection of STOP Condition
* Supported generation and detection of Repeated START Condition
* Detection of the busy state of the highway is supported
* All registers are 32 bit width
* Supported logic for generating and controlling interrupt signals
* Supported only half-duplex communication
* Supported detection of arbitration lost and NACK bit
* Maximum system clock speed is ... MHz
* Communication speeds according to the following standard are supported*: Fast M*ode Plus *1MHz,* Fast-Mode *400kHz i* Standard Mode *100kHz*
* Supported generation of GPO (General Purpose Output) signal which width is 1 – 8 bits
* Supported 7 bits and 10 bits slave address length
* Minimum system clock speed is 1 MHz
* Operating temperature 0 – 85
* ....
* ...

# **Detailed architecture**



**Image 1. Detailed architecture of the Wisbone I2C IP Core.**

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**Image 2. System architecture verification.**

# **Wishbone I2C IP Core – Signals**

This section contains description of all the signals that are necessary for connecting Wishbone I2C IP Core to other devices.

## **Wisbone Signals**

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal name** | **Width** | **Type** | **Description** |
| clk\_i | 1 | Input | System clock |
| addr\_i | 8 | Input | Adress of register |
| we\_i | 1 | Input | Enable write to registers |
| rst\_i | 1 | Input | Reset signal |
| dat\_i | 32 | Input | Input Data |
| dat\_o | 32 | Output | Output Data |
| int | 1 | Output | Interrrupt signal |
| ack\_o | 1 | Output | Acknowledgne signal |
|  |  |  |  |

## **I2C Interface Signals**

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal name** | **Width** | **Type** | **Description** |
| SCL | 1 | Inout | Serial Clock Line |
| SDA | 1 | Inout | Serial Data Line |
| GPO | 1-8 | Output | General Purpose Output |
|  |  |  |  |

# **Registers**

This section contains explanation about Wishbone I2C IP Core registers and their parameters that user can configure according to their needs.

|  |  |  |  |
| --- | --- | --- | --- |
| **Register name** | **Address** | **Width** | **Description** |
| Tx Register | 0x00 | 32 | Transmit data register |
| Rx Register | 0x01 | 32 | Receive data register |
| Control Register | 0x02 | 32 | Control register |
| Status Register | 0x03 | 32 | Status register |
| Command Register | 0x04 | 32 | Command register |
| Slave Address | 0x05 | 32 | Slave address register |
| GPO Register | 0x06 | 32 | General Purpose Output register |
| System Clock Register | 0x07 | 32 | System Clock register |
|  |  |  |  |

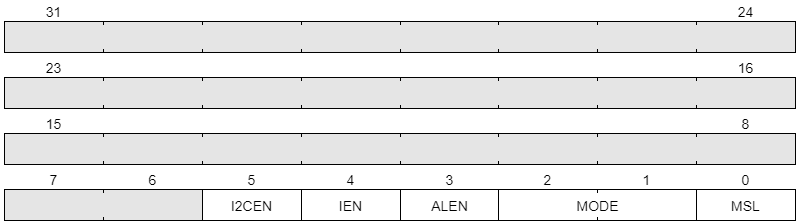
Tx Register contains data for transmit. In this register only 8 down bits are valid.

Rx Register containt received data. In this register only 8 down bits are valid.

GPO (General Purpose Output) register containt data which will be send on GPO. In this register only 1-8 down bits are valid. Number of valid bits is configurable.

## **Control Register**

Control register allows to enale I2C communication, enable interrupt, select speed mode, select master or slave mode and choice slave address length (7 or 10 bits).



Bit 5 -> **I2CEN** : I2C Enable

1 – I2C Enabled

0 – I2C Disabled

Bit 4 ->  **IEN** : Interrupt Enable

1 – Interrupt Enabled

0 – Interrupt Disabled

Bit 3 -> **ALEN**: Slave Address Length

1 – 10 bit adress

0 – 7 bit adress

Bit 2:1 -> **MODE**: Mode Select

00 – Standard Mode 100 KHz

01 – Fast Mode 400 KHz

10 – Fast Plus Mode 1 MHz

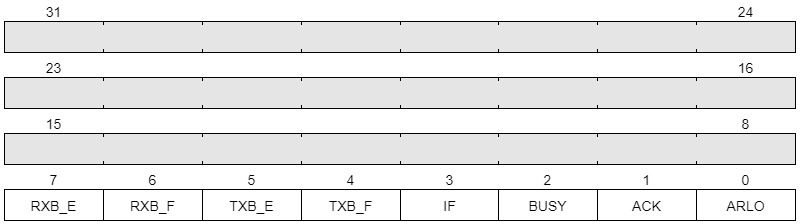
Bit 0 -> **MSL** : Master/slave select

0 – Master

1 – Slave

## **Status Register**

Status register is read only register. User can only read info data from this register.



Bit 7 -> **RXB\_E**: Rx Buffer Empty

1 – Rx Buffer Empty

0 – Rx Buffer Not Empty

Bit 6 -> **RXB\_F**: Rx Buffer Full

1 – Rx Buffer Full

0 – Rx Buffer Not Full

Bit 5 -> **TXB\_E**: Tx Buffer Empty

1 – Tx Buffer Empty

0 – Tx Buffer Not Empty

Bit 4 -> **TXB\_F**: Tx Buffer Full

1 – Tx Buffer Full

0 – Tx Bufffer Not Full

Bit 3 -> **IF**: Interrupt Flag

1 – Interrupt detected

0 – Interrupt not detected

Bit 2 -> **BUS**Y: Indicates That I2C Bus is Busy

1 – Start Condition Detected

0 – Stop Condition Detected

Bit 1 -> **ACK**: RxACK

1 – No ACK Received

0 - ACK Received

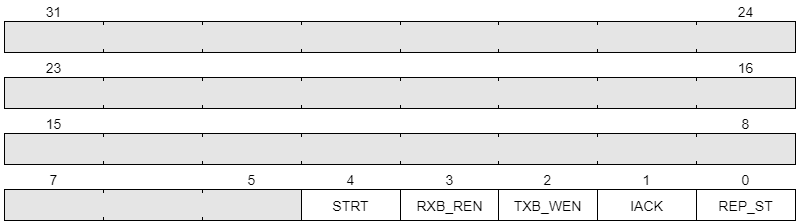
Bit 0 -> **ARLO**: Arbitration Lost

1 – STOP is detected but not requested, Master drives SDA HIGH but SDA is LOW

0 - No Arbitration Lost

## **Command Register**

Command register is read/write register.



Bit 4 -> **STRT**: Start I2C Transaction

Bit 3 -> **RXB\_REN**: Rx Buffer Read Enable

Bit 2 -> **TXB\_WEN**: Tx Buffer Write Enable

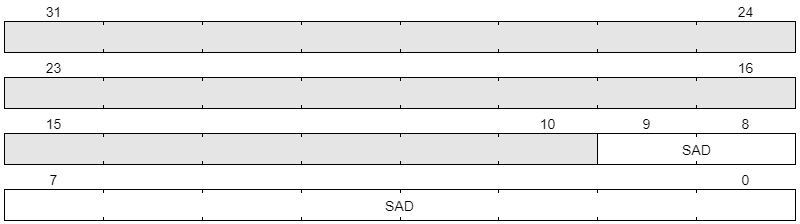
Bit 1 -> **IACK**: Clear pending Interrupt

Bit 0 -> **REP\_ST**: Repeated Start

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## **Slave Address Register**

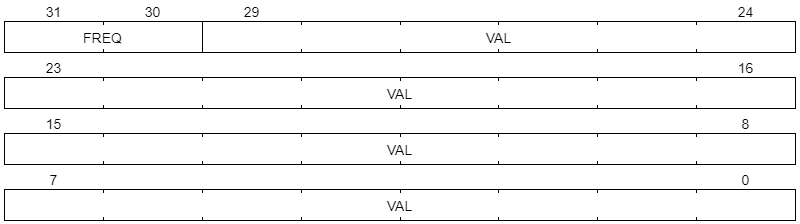
Slave Address Register contains device address when Wishbone I2C IP Core is in slave mode.



Bit 9:0 -> **SAD**: Slave Address

## **System Clock Register**

System Clock Register contains info about system clock value in Hz.



Bit 31:30 -> **FREQ**: Signal Frequency

00 – Hz

01 – KHz

10 – MHz

11 – GHz

Bit 29:0 -> **VAL:** Clock Signal Value in The Aforementioned Frequency